IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1, 10, 17-18, and 22-29 in accordance with the following:

1. (CURRENTLY AMENDED) A processor control apparatus for controlling a plurality of arithmetic units, said processor control apparatus, comprising:

a plurality of instruction control units issuing a series of instructions to said plurality of arithmetic units,

wherein at least one of said instruction control units switches between a first execution process driving said plurality of arithmetic units by a single series of instructions issued from a single one of the plurality of instruction control units and the plurality of arithmetic units execute the single series of instructions concurrently both upon the single series of instruction including different commands for each of the plurality of instruction control units and the single series of instructions including a same command for each of the plurality of instruction control units, and a second execution process correspondingly driving said plurality of arithmetic units by a plurality of different series of instructions issued respectively from more than one of said plurality of instruction control units and in which the processing by the plurality of arithmetic units can be synchronized.

2. (PREVIOUSLY PRESENTED) The processor control apparatus according to claim 1, wherein said at least one instruction control unit each perform a switching process switching between said first execution process and said second execution process according to information which is contained in advance in a series of instructions.

3. (ORIGINAL) The processor control apparatus according to claim 1,

wherein when an M-th one of said instruction control units issues a second series of instructions to an N-th one of said arithmetic units which is performing said second execution process based on a first series of instructions issued by an N-th one of said instruction control units different from said M-th instruction control unit, said M-th instruction control unit is set in a wait state until said N-th arithmetic unit completes said second execution process.

4. (ORIGINAL) The processor control apparatus according to claim 1, further comprising a first storage element for holding a plurality of series of instructions,

wherein when an M-th one of said instruction control units issues a second series of instructions to an N-th one of said arithmetic units which is performing said second execution process based on a first series of instructions issued by an N-th one of said instruction control units different from said M-th instruction control unit, said second series of instructions from said M-th instruction control unit are stored in said first storage element, and

wherein said N-th arithmetic unit executes instructions which are stored in said first storage element based on information contained in said first series of instructions issued by said N-th instruction control unit.

5. (PREVIOUSLY PRESENTED) The processor control apparatus according to claim 1, further comprising a second storage element which operates to hold, when one of said arithmetic units executing a first series of instructions from one of said instruction control units is switched to execute a second series of instructions from another instruction control unit, data generated by the second series of instructions under execution by associating the data with that instruction control unit which is executing the second series of instructions.

6. (ORIGINAL) The processor control apparatus according to claim 1,

wherein it is determined, based on an instruction executing state of each arithmetic unit, one of said arithmetic units to which a new series of instructions is to be issued by one of said instruction control units, and

wherein said one instruction control unit is controlled based on the result of the determination so that the new series of instructions are directed to said one arithmetic unit thus determined.

7. (ORIGINAL) The processor control apparatus according to claim 1,

wherein each of said series of instructions includes a VLIW type instruction.

8. (ORIGINAL) The processor control apparatus according to claim 1,

wherein each of said series of instructions includes a series of time sharing instructions for serially driving a plurality of ones of said arithmetic units.

9. (ORIGINAL) The processor control apparatus according to claim 1, further

comprising power control elements for controlling power supply to said arithmetic units based on their instruction executing states.

10. (CURRENTLY AMENDED) A processor control apparatus, comprising:

a plurality of instruction memories for storing a plurality of series of instructions to be executed by a plurality of arithmetic units;

an instruction decoder for decoding a series of instructions from said instruction memories, and outputting a decoded result to any of said plurality of arithmetic units; and

a selector for selectively switching between a plurality of series of instructions from said instruction memories to be decoded by said instruction decoder, and supplying a series of instructions thus selected to said instruction decoder,

wherein said plurality of series of instructions are issued to said plurality of arithmetic units from both a single one of the plurality of instruction memories ~~or are~~ and issued respectively from more than one of said plurality of instruction memories to enable said plurality of arithmetic units to be simultaneously and independently driven.

11. (ORIGINAL) The processor control apparatus according to claim 10,

wherein some of said plurality of series of instructions contain information about selective switching between said series of instructions to be performed by said selector, and

wherein said instruction decoder decodes said information contained in a series of instructions, and outputs a switching instruction to said selector.

12. (ORIGINAL) The processor control apparatus according to claim 10,

wherein some of said plurality of series of instructions contain a synchronizing instruction for allowing a first predetermined one of said arithmetic units and a second predetermined arithmetic unit to synchronously perform processes, and

wherein when said synchronizing instruction is issued to said first predetermined arithmetic unit, said first predetermined arithmetic unit is set in a wait state, and an instruction decoder of said second predetermined arithmetic unit does not output a switching instruction to its associated selector if a process is being executed by said second predetermined arithmetic unit upon issuance of said synchronizing instruction, and does not release the wait state of said first predetermined arithmetic unit until said second predetermined arithmetic unit completes said process.

13. (ORIGINAL) The processor control apparatus according to claim 10, further comprising:

an instruction queue for temporarily storing, at a stage prior to said selector, a series of instructions to be transmitted from a second one of said instruction memories different from a first one of said instruction memories which stores a series of instructions being executed by said first predetermined arithmetic unit; and

a determiner for determining, based on a series of instructions being executed, whether or not the process being performed by said first predetermined arithmetic unit can be interrupted, said determiner operating to output, if the process can be interrupted, an interrupt signal for interrupting the issuance of the series of instructions to said first instruction memory which is a source of the series of instructions being executed, and generate a switching instruction to said selector to switch to a series of instructions from said instruction queue.

14. (ORIGINAL) The processor control apparatus according to claim 10,

wherein each of said series of instructions includes a VLIW type instruction.

15. (ORIGINAL) The processor control apparatus according to claim 10,

wherein each of said series of instructions includes a series of time sharing instructions for serially driving a plurality of ones of said arithmetic units.

16. (ORIGINAL) The processor control apparatus according to claim 10, further comprising power control elements for controlling power supply to said arithmetic units based on their instruction executing states.

17. (CURRENTLY AMENDED) A processor control apparatus, comprising:

a single instruction memory for storing a plurality of series of instructions to be executed by a plurality of arithmetic units;

an instruction decoder decoding a series of instructions from said instruction memory, and outputting a decoded result to any of said plurality of arithmetic units; and

a selector selectively switching between a plurality of series of instructions from said instruction memory to be decoded by said instruction decoder, and supplying a series of instructions thus selected to said instruction decoder;

wherein said instruction memory has a plurality of ports for issuing said series of instructions to said instruction decoder.

wherein said plurality of series of instructions are issued to said plurality of arithmetic units from the instruction memory to be simultaneously and independently driven both upon the instructions including different commands for each of the plurality of instruction control units and including a same command for each of the plurality of instruction control units.

18. (CURRENTLY AMENDED) A processor control apparatus for controlling a plurality of arithmetic units, said processor control apparatus comprising:

a plurality of instruction control units for instructing said arithmetic units to execute a series of instructions, wherein each of said instruction control units ~~includes~~ comprises:

an instruction memory for storing a plurality of series of instructions; and

an instruction decoder for decoding a series of instructions and supplying the decoded series of instructions to an associated one of said arithmetic units, and wherein some of said instruction control units each have an instruction control selector for selectively switching between a first series of instructions from a first instruction memory of one of said instruction control units for simultaneously driving the plurality of arithmetic units both upon the instructions including different commands for each of the plurality of instruction control units and including a same command for each of the plurality of instruction control units and a second series of instructions from a second instruction memory of another instruction control unit different from said one instruction control unit for independently driving each of the plurality of arithmetic units to output one of said first and second series of instructions thus selected to said instruction decoder,

wherein each of said arithmetic units ~~includes~~ comprises:

a first register file and a second register file for storing data generated by said first and second series of instructions, respectively, which are supplied from said first and second instruction memories and decoded by an instruction decoder of an associated one of said instruction control units; and

an arithmetic unit selector for selectively switching between said data generated by said first and second series of instructions being executed and stored in said first and second register files, respectively, according to an instruction from said associated instruction decoder to supply a selected one of said first and second series of instructions to a calculator.

19. (ORIGINAL) The processor control apparatus according to claim 18, wherein each of said series of instructions includes a VLIW type instruction.

20. (ORIGINAL) The processor control apparatus according to claim 18,

wherein each of said series of instructions includes a series of time sharing instructions for serially driving a plurality of ones of said arithmetic units.

21. (ORIGINAL) The processor control apparatus according to claim 18, further comprising power control elements for controlling power supply to said arithmetic units based on their instruction executing states.

22. (CURRENTLY AMENDED) A processor control apparatus for controlling a plurality of arithmetic units, said processor control apparatus comprising:

a plurality of instruction control units for instructing said arithmetic units to execute a series of instructions,

wherein said instruction control units have a single instruction memory used in common for storing a plurality of series of instructions, and each ~~includes~~ comprises an instruction decoder for decoding a series of instructions and supplying the decoded series of instructions to an associated one of said arithmetic units, and said single instruction memory has a plurality of ports for issuing said series of instructions to said respective instruction decoders,

wherein some of said instruction control units each ~~having~~ comprising an instruction control selector for selectively switching between a first series of instructions simultaneously driving the plurality of arithmetic units both upon the instructions including different commands for each of the plurality of instruction control units and including a same command for each of the plurality of instruction control units and a second series of instructions independently driving each of the plurality of arithmetic units both from said single instruction memory to output one of said first and second series of instructions thus selected to said instruction decoder,

wherein each of said arithmetic units ~~includes~~ comprises:

a first register file and a second register file for storing data generated by said first and second series of instructions, respectively, which are supplied from said single instruction memory and decoded by an instruction decoder of an associated one of said instruction control units; and

an arithmetic unit selector for selectively switching between said data generated by said first and second series of instructions being executed and stored in said first and second register files, respectively, according to an instruction from said associated instruction decoder to supply a selected one of said first and second series of instructions to a calculator.

23. (CURRENTLY AMENDED) A processor, comprising:

a plurality of arithmetic units; and

a plurality of instruction control units for issuing a series of instructions to drive said arithmetic units in a controlled manner;

wherein some of said instruction control units are operable to switch between a first execution process for ~~synchronous~~ synchronously driving said plurality of arithmetic units by a single series of instructions both upon the instructions including different commands for each of the plurality of instruction control units and including a same command for each of the plurality of instruction control units and a second execution process independently driving said plurality of arithmetic units by a plurality of different series of instructions, respectively, ~~wherein the synchronous driving and the independent driving~~.

24. (CURRENTLY AMENDED) A processor, comprising:

a plurality of arithmetic units;

a plurality of instruction memories for storing a plurality of series of instructions to be executed by said plurality of arithmetic units;

an instruction decoder for decoding a series of instructions from said instruction memories, and outputting a decoded result to any of said plurality of arithmetic units; and

a selector for selectively switching between a plurality of series of instructions from said instruction memories to be decoded by said instruction decoder, and supplying a series of instructions thus selected to said instruction decoder

wherein said plurality of series of instructions are issued to said plurality of arithmetic units from one of the plurality of instruction memories or are issued respectively from said plurality of instruction memories to enable said plurality of arithmetic units to be simultaneously and independently driven, and the plurality of arithmetic units execute the single series of instructions concurrently both upon the single series of instructions including different commands for each of the plurality of instruction control units and the single series of instructions including a same command for each of the plurality of instruction control units.

25. (CURRENTLY AMENDED) A processor, comprising:

a plurality of arithmetic units;

a single instruction memory for storing a plurality of series of instructions to be executed by said plurality of arithmetic units;

an instruction decoder for decoding a series of instructions from said instruction memory,

and outputting a decoded result to any of said plurality of arithmetic units; and

a selector for selectively switching between a plurality of series of instructions from said instruction memory to be decoded by said instruction decoder, and supplying a series of instructions thus selected to said instruction decoder;

wherein said instruction memory has a plurality of ports for issuing said series of instructions to said respective instruction decoders,

wherein said plurality of series of instructions are issued to said plurality of arithmetic units from the instruction memory to be simultaneously and independently driven, and the plurality of arithmetic units execute the single series of instructions concurrently both upon the single series of instruction including different commands for each of the plurality of instruction control units and the single series of instructions including a same command for each of the plurality of instruction control units.

26. (CURRENTLY AMENDED) A processor, comprising:

a plurality of arithmetic units;

a plurality of instruction control units for driving said arithmetic units in a controlled manner,

wherein each of said instruction control units ~~includes~~ comprises:

an instruction memory for storing a plurality of series of instructions; and

an instruction decoder for decoding a series of instructions and supplying the decoded series of instructions to an associated one of said arithmetic units, and

wherein some of said instruction control units each have an instruction control selector ~~for~~ selectively switching between a first series of instructions from a first instruction memory of one of said instruction control units simultaneously driving the plurality of arithmetic units and a second series of instructions from a second instruction memory of another instruction control unit different from said one instruction control unit independently driving each of the plurality of arithmetic units to output one of said first and second series of instructions thus selected to said instruction decoder, based on contents of processes to be executed,

wherein each of said arithmetic units ~~includes~~ comprises:

a first register file and a second register file for storing data generated by said first and second series of instructions, respectively, which are supplied from said first and second instruction memories and decoded by an instruction decoder of an associated one of said instruction control units; and

an arithmetic unit selector for selectively switching between said data generated

by said first and second series of instructions being executed and stored in said first and second register files, respectively, according to an instruction from said associated instruction decoder to supply a selected one of said first and second series of instructions to a calculator, and the plurality of arithmetic units execute the single series of instructions concurrently both upon the single series of instructions including different commands for each of the plurality of instruction control units and the single series of instructions including a same command for each of the plurality of instruction control units.

27. (CURRENTLY AMENDED) A processor, comprising:

a plurality of arithmetic units;

a plurality of instruction control units driving said arithmetic units in a controlled manner,

wherein said instruction control units have a single instruction memory used in common for storing a plurality of series of instructions, and each ~~includes~~ comprises an instruction decoder for decoding a series of instructions and supplying the decoded series of instructions to an associated one of said arithmetic units, and said single instruction memory has a plurality of ports for issuing said series of instructions to said respective instruction decoders,

wherein some of said instruction control units each having an instruction control selector for selectively switching between a first series of instructions simultaneously driving the plurality of arithmetic units both upon the instructions including different commands for each of the plurality of instruction control units and including a same command for each of the plurality of instruction control units and a second series of instructions independently driving each of the plurality of arithmetic units both from said single instruction memory to output one of said first and second series of instructions thus selected to said instruction decoder, based on contents of processes to be executed,

wherein each of said arithmetic units ~~includes~~ comprises:

a first register file and a second register file for storing data generated by said first and second series of instructions, respectively, which are supplied from said single instruction memory and decoded by an instruction decoder of an associated one of said instruction control units; and

an arithmetic unit selector for selectively switching between said data generated by said first and second series of instructions being executed and stored in said first and second register files, respectively, according to an instruction from said associated instruction decoder to supply a selected one of said first and second series of instructions to a calculator.

28. (CURRENTLY AMENDED) A processor controlling method usable with a plurality of instruction control units for controlling a plurality of arithmetic units to execute a plurality of series of instructions, said method comprising:

prescribing, in advance in a series of instructions which is to be performed, synchronous execution in which a plurality of predetermined ones of said arithmetic units are synchronously driven by a single series of instructions, or independent execution in which the plurality of predetermined arithmetic units are independently driven by a plurality of respective series of instructions; and

switching between the synchronous driving both upon the instructions including different commands for each of the plurality of instruction control units and including a same command for each of the plurality of instruction control units and the independent driving of the predetermined arithmetic units for performing a series of instructions based on the contents of the prescription therein.

29. (CURRENTLY AMENDED) A processor control method to control a plurality of arithmetic units connected with a plurality of instruction control units, comprising:

switching between simultaneously driving the plurality of arithmetic units by issuing a single series of instructions from one of the plurality of instruction control units both upon the instructions including different commands for each of the plurality of instruction control units and including a same command for each of the plurality of instruction control units and independently driving each of the plurality of arithmetic units by correspondingly issuing series of instructions from the plurality of instruction control units, wherein the switching is performed based on contents of processes to be executed.